UCD3138 - Practical Design Guideline

High Power Controllers Solution

1. **Introduction**

There are multiple grounds and bias power pins for a digital controller, such as UCD3138. They are separated from each other because of digital circuitry and analog circuitry inside the device. Normally, digital circuits draw more current and generate more noise, but the digital signal is not sensitive to the noise; while the analog circuit needs a quiet power and grounding. A deliberate grounding and power separation outside the controller can reduce the interference between analog circuit and digital circuit, and the controller can have better performance. When they are separated from each other, care must be taken on how the analog circuit is grouped together and digital circuit is grouped together, and then how and where they are tied together. With improper grounding, the device performance can be negatively impacted including device reset, ADC results, output voltage ripple.

In the PCB design, there are two options. One is to have two separate grounds, i.e., digital ground and analog ground. The other is to use a single ground plane for both digital ground and analog ground. With two separate ground planes, how to connect digital ground and analog ground is very important and PCB must be designed very carefully. With a single ground plane, there is no worry about where two grounds are tied together, and it makes PCB design much easier. Here, we recommend to use a single ground plane.

In this document, digital ground is denoted as DGND; analog ground is denoted as AGND; a single ground plane is denoted as SGND.

1. **UCD3138 Pin Connection Recommendation**

UCD3138 is a highly integrated controller with a large number of mixed signals. It is important to group each pin, select good components and have appropriate connection to each pin, and make good placement on the PCB in order to reduce noise coupling and prevent chip mal-function. First, group all digital circuitry and analog circuitry, and second, place digital circuitry close to each other, then place analog circuitry close to each other, then finally make trace connections among them. To achieve a robust design, at least 4-layer board is strongly recommended.

Next, layout considerations and examples are provided for some critical pins or signals.

**1). /RESET Pin:**

/RESET pin should have one at least 2.2µF low ESL capacitor locally decoupled with DGND plane or SGND plane. As shown in Fig. 1, this capacitor must be located very close to the device/RESET pin. It is highly recommended to use a small resistance (such as 220 Ω) to connect the /RESET pin (Pin 11 in UCD3138RGC) with V33DIO (Pin 9 in UCD3138RGC). The resistor should be placed close to the /RESET pin as well. The grounding point of the capacitor should be close to DGND plane or SGND plane.

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SGND or DGND Via

Reset Capacitor

Reset Resistor

(Use 220 Ohm)

Reset Trace

Figure 1. /Reset pin connection

**2). ADC Pins**

Use low ESL/ESR ceramic capacitors on ADC pins to decouple with AGND or SGND. The capacitor value is selected such that the cut-off frequency is one tenth the sampling frequency if there is no dynamic requirement. This can help keep down noise coupled during signal transmission.

ADC input is a single-ended signal, if the sensing trace is long, move it away from radiation sources and add shielding between the signal and the radiation sources.

**3). EAP and EAN Pins**

They are dual-ended sensing input circuit with good common mode noise rejection. Keep the distance between the two traces as short as possible. A local filter close to the EAP/EAN pins is required as shown in Figure 2; C1 is added to filter out the common mode noise on the sensing line and make the sensing voltage stable. The capacitor is connected to AGND or SGND if a single plane is used.



Figure 2. Local filter on EAPx/EANx pins

**4). Current Amplifier with EADC Connection**

When a current amplifier is used for current sensing, it is referenced to DGND, then followed by LPF which is referenced to AGND, as shown in Figure 3. LPF should be placed close to the device. If a single plane is used, both filters should be connected to the same ground plane (SGND).



Figure 3. Current amplifier connected with EADC

**5). Communication Ports Including I2C, UART and SPI**

UART and I2C are used for communicating with other devices. Normally, the communication wires are long. These wires can easily be polluted by EMI and pick up noise in switching power supplies. First, the wires must be routed without directly exposing the traces to switching noise source, then a termination is needed at the end of the wire, as shown in Figure 4. For example, R = 50Ω, C = 47pF if it does not significantly slow down the slew rate of the signals. Since SPI is local communication port and the trace is normally short, termination is not needed. When the pins are not used, tie them to a single ground plane SGND or DGND if there are two separate ground planes.



Figure 4. Termination for communication port (e. g., UART)

**6). DPWM Pins**

If DPWMs travel for a longer distance than 3 inches from the control card to a main power stage, a clamping diode may be needed as shown in Figure 5 to prevent electrical overstress on the device. The fast switching current can generate noises to other circuits and may also pick up the noises from other switching source. Avoid DPWM signals to cross switching nodes. DPWM has a reference of DGND or SGND.



Figure 5. Clamping diode for DPWM

**7). GPIOs**

GIPO is referenced to DGND internally. When GPIO pins are not used, connect the pins to DGND/SGND. Alternatively, they can be configured as output pins and set as low in the firmware. When GPIOs are used to drive other circuit like LED, be aware that it can pick up noise. A local resistor close to UCD3138 is used to terminate the coupled noise. If the big voltage swings, a clamping diode is needed as shown in Figure 6. The clamping diodes are connected to DGND or SGND.



Figure 6. Clamping diode for GPIO

**8). Bias Supply and Grounding**



Figure 7. 3.3V and grounding connection diagram (64 pins)

+3.3Vbias normally is produced by LDO or Buck converter. Figure 7 is a block diagram of the UCD3138RGC (64-Pin device) that depicts how the pins are connected. +5V or +12V normally are generated by a flyback converter and it is referenced to the Power Return. A 10µF capacitor is locally used for LDO or buck between +3.3V and Power Return. From there, use a single plane (SGND) for both digital ground and analog ground. A 1Ω resistor is needed between V33D and V33A. As an example, a 4.7µF decoupling capacitor is used for V33A and V33D respectively and these decoupling capacitors should be placed close to the device pins. In addition, a 0.1µF capacitor is used for V33A and V33D respectively to filter out the high frequency noise. 1µF decoupling capacitor is used for V33DIO. If DGND and AGND are separated, then the decoupling capacitor of V33A should be connected to AGND, and the decoupling capacitor of V33D should be connected to DGND. A small current return loop is important to reduce return impedance. There should not be any voltage level shift between internal DGND and internal AGND. Multiple vias are required to connect the extended Power pad (i.e., copper under the device power pad) to the internal single ground (SGND) plane layer. All digital or analog ground pins can be directly connected to the extended power pad or connected to the internal SGND plane through vias. If DGND and AGND planes are separated, extended power pad needs to be connected to AGND plane.

**9). BP18**

Except UCD3138128, UCD3138A64 and UCD3138A, BP18 decoupling capacitors MUST be connected on all other UCD family. 1µF and 0.1µF capacitors are used between BP18 and SGND, as shown in Fig. 7. As recommended in UCD3138 datasheet, connect a 2.2µF capacitor between V33D to BP18. They should be placed close to the device pin, and keep the return loop as small as possible.

In the UCD3138128, UCD3138A64, and UCD3138A, there is no need for 2.2µF capacitor between V33D and BP18 due to internal circuit enhancement which eliminates the GPIO short pulse during V33D ramp up.

**10). A Layout Example for The Device UCD3138A**



Figure 8. A layout example on top layer



Figure 9. A layout example on ground layer

**10). DPWMs Synchronization**

For half bridge or full-bridge converter, where more than one DPWM modules are used to drive multiple pairs of MOSFETs, the synchronization between DPWM modules is strongly recommended. The synchronization can be achieved by using Master-Slave mode. A slaved DPWM can be synchronized with other Master DPWM or Slave DPWM. Without synchronization, the DPWM could go out of synchronization at large currents which can cause catastrophic damage.

**11). Auxiliary Supply Power Transformer Shielding**

Auxiliary supply normally adopts a flyback converter, and its power transformer can generate large electromagnetic field which can interfere with other electronic circuitry. By shielding the primary side windings, the EMI can be effectively reduced so that the surrounding circuit can have quiet working environment.

1. **EMI/EMC Mitigation Guideline**

Every design is different in terms of EMI/EMC mitigation, and it requires its own solution.

* Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, capacitance and ESR, and they have different frequency response;
* Avoid long traces close to radiation sources, and place them into an internal layer. It is preferred to have ground shielding and add a termination circuit at the end of the trace;
* Single ground is recommended: SGND. A multilayer such as 4 layers board is recommended so that one solid SGND is dedicated for return current path;
  + - Use one whole layer (L3) for SGND plane as shown in Figure 10. Use many vias (such as 16 vias) to connect the extended power pad to the internal SGND plane layer. It is preferred to have the vias close to AGND pins and DGND pins of the device. For the 80-pin device, since there is no power pad, add a ground plane under the device;
    - Place the UCD3138 controller away from radiation or switching components, then layer 2 is used for trace routing to achieve good shielding from the ground layer (L3), as shown in Figure 10;



Figure 10. Ground layer assignment option 1

* Add low pass filter on analog signals close to the header connecting the control card and the power board;
* Analog circuit such as ADC sensing lines needs a return current path into the analog plane; digital circuit such as GPIO, PMBus and PWM has a return current path into the digital plane; With a single plane, one should still try to avoid mixing analog current and digital current;
* Don’t use the ferrite bead to connect V33A and V33D;
* Avoid negative current/negative voltage on all pins, so Schottky diodes may be needed to clamp the voltage; avoid the voltage spike on all pins to exceed 3.8V or below -0.3V; add Schottky diodes on the pins which could have voltage spikes during surge test; be aware that Schottky diode has relatively higher leakage current, which can affect the voltage sensing at high temperature.

1. **Special Considerations**

* The first thing that should be done in any layout is to set up the basic grounding strategy and the placement of the decoupling capacitors. This needs to be prioritized over anything else even the routing of sensitive feedback signals;
* If there are separate AGND or DGND planes, they should be tied together close to the chip;
* If a gate driver device such as UCC27524 or UCC27511 is on the control card and there is a PGND connection, a net-short resistor or large copper trace should be used to tie the PGND to the Power RTN by multiple vias. In addition, the net-short element between Power RTN and PGND should be close to the driver IC;
* Avoid V33D and V33A long trace or plane close to radiation components, and place them into an internal layer, and it is preferred to have ground shielding;
* Avoid bias supplies or SGND or Power RTN directly to cross switching power train, where they can couple switching noises. If the grounds are coupled with noises, the decoupling capacitors may not be effective to filter the noise out.
* Local capacitors are preferred to provide a short path for switching current, and be careful to select a quiet RETURN point to connect;
* In power module or a tiny PCB design, a single solid plane without the grounding separation is shown in Figure 11, and they have a single point connection with power RTN or SGND near the connector. Make sure there is no current flow from power train into the signal ground plane.



Figure 11. A single ground plane for module design